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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/829,793	04/10/2001	Martijn Johannes Lambertus Emons	NL 000215	1893

24738 7590 11/04/2004

PHILIPS ELECTRONICS NORTH AMERICA CORPORATION
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EXAMINER	
KIM, HONG CHONG	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 11/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action	Application No.	Applicant(s)	
	09/829,793	EMONS, MARTIJN JOHANNES LAMBERTUS	
	Examiner	Art Unit	
	Hong C Kim	2186	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 05 October 2004 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

a) ☐ The period for reply expires _____months from the mailing date of the final rejection.

b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection. ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1.☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.

2.☒ The proposed amendment(s) will not be entered because:

(a) ☒ they raise new issues that would require further consideration and/or search (see NOTE below);

(b) ☐ they raise the issue of new matter (see Note below);

(c) ☒ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

(d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: *See Continuation Sheet*.

3.☐ Applicant's reply has overcome the following rejection(s): _____.

4.☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

5.☐ The a)☐ affidavit, b)☐ exhibit, or c)☐ request for reconsideration has been considered but does NOT place the application in condition for allowance because: _____.

6.☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.

7.☐ For purposes of Appeal, the proposed amendment(s) a)☐ will not be entered or b)☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

The status of the claim(s) is (or will be) as follows:

Claim(s) allowed: _____.

Claim(s) objected to: _____.

Claim(s) rejected: *6-8*.

Claim(s) withdrawn from consideration: _____.

8.☐ The drawing correction filed on _____ is a)☐ approved or b)☐ disapproved by the Examiner.

9.☐ Note the attached Information Disclosure Statement(s)(PTO-1449) Paper No(s). _____.

10.☒ Other: *attachement*

Continuation of 2. NOTE: It appears that the added limitations raise new issues and would requir further consideration and search. Also cache bypass instruction being executed by a processor is well known in the memory art (i.e USP 5875464) .

HONG CHONG KIM
PRIMARY EXAMINER

09/829,793

Attachement

US-PAT-NO: 5875464

DOCUMENT-IDENTIFIER: US 5875464 A
See Image for Certificate of Correction

TITLE: Computer system with private and shared partitions in cache

DATE-ISSUED: February 23, 1999

US-CL-CURRENT: 711/129, 711/121 , 711/173

APPL-NO: 08/ 617347

DATE FILED: March 18, 1996

PARENT-CASE:

The application is a continuation, of application Ser. No. 08/400,300, filed Mar. 6, 1995, abandoned, which is a continuation of application Ser. No. 07/805,406, filed Dec. 10, 1991, now abandoned.

------ KWIC ------

US Patent No. - PN (1):
5875464

Detailed Description Text - DETX (46):
A similar approach can be used in exploiting the program knowledge available to the compiler to enhance the performance and predictability of cache based memory systems. Processors which support cache control instructions such as cache flush, cache bypass and cache freeze can use compiler support to determine the optimal placement of these cache instructions. Compiler support includes: identifying frequently executed loops for freezing in cache; identifying random data accesses for cache bypass to avoid "pollution"; providing memory reference dispersion to minimize intra-task cache line collisions in multi-tasking environments; and the control of cache line replacement (rather than by LRU, etc.). The investigation of compiler-aided cache performance enhancements is discussed in detail by Chi in Compiler Driven Cache Management using a State Level Transition Model. PhD thesis, Purdue University, December, 1989. EE 89-71.

Detailed Description Text - DETX (59):
While this approach can provide significantly better performance than the simple cache locking technique presented in the previous section, it suffers from two major drawbacks. First, shared data structures can not be kept in cache if internal cache coherence is to be guaranteed. ELXSI addresses this